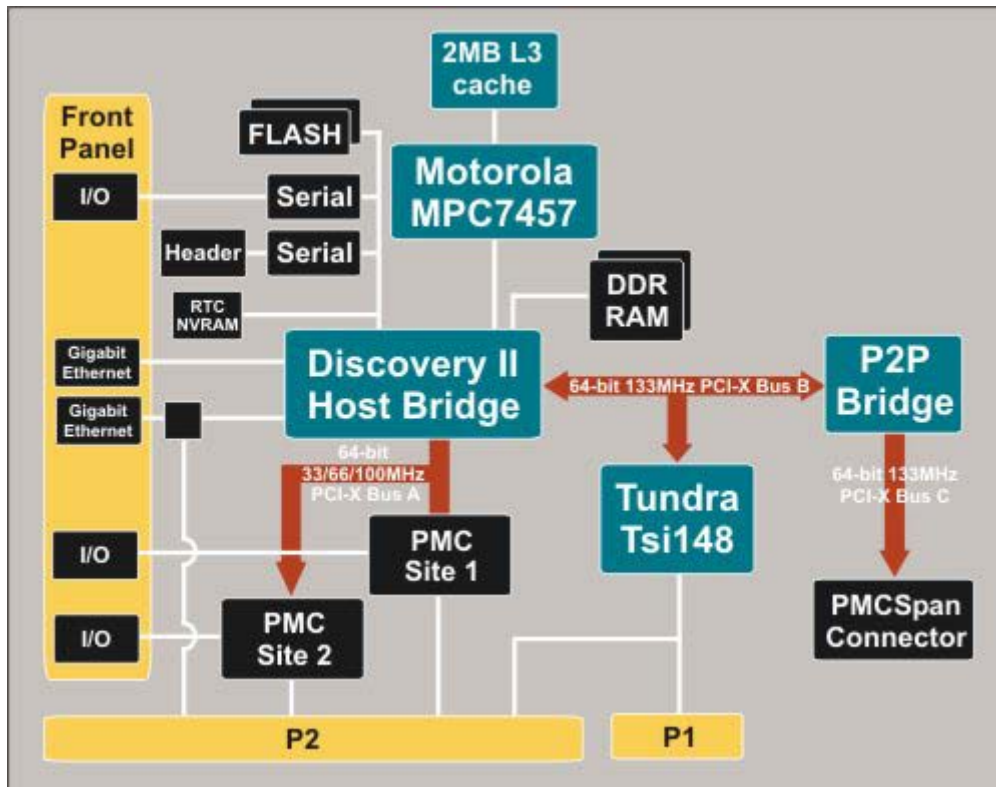


# MOTOROLA'S MVME6100 THE FIRST VME RENAISSANCE MASTERPIECE

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At the Bus & Boards Show in January 2002, Motorola announced the beginning of the VME Renaissance, a period of increased intellectual activity and technology insertion surrounding the VMEbus, an era of innovation and performance improvement with preservation of backward compatibility and protection of legacy customer investments. The newest milestone in the VME Renaissance is the introduction of the Motorola MVME6100 single board computer (SBC). The MVME6100 provides users with significant increases over previous product generations in the areas of CPU, memory, and VME/PCI I/O performance in a variety of applications such as Defense & Aerospace, Industrial Automation, and Medical Imaging. This article explores the details of this powerful new single board computer.

Refer to the Block Diagram of the MVME6100 in Figure 1 throughout this article.



## Processor and Caches

The MVME6100 utilizes the Motorola MPC7457 Processor, a high-performance, lower-power 32-bit implementation of the PowerPC™ RISC architecture with a full 128-bit implementation of Motorola's AltiVec™ technology. The core clock frequency is 1.267 GHz with a core voltage of 1.3V. The processor has 8-way set-associative 32KByte on-chip L1 data and instruction caches that operate at the core clock frequency. The MPC7457 processor also has an 8-way set-associative 512KB on-chip L2 cache, twice as much as the MPC7455 processor's L2 cache. The L2 cache operates at the core clock frequency as well. The processor also provides an external SRAM interface that can be configured to support either 2 MB of backside 8-way set-associative L3

cache or 2 MB of private memory. When the 2 MB of SRAM is configured as private memory, it can be utilized as high-speed memory by the processor. Private memory has lower access latency than system memory since accesses do not have to be arbitrated on the processor bus and pass through the Discovery II™ system controller. The L3 cache/private memory is implemented using two 8-megabit DDR SRAM devices operating at 200 MHz. The MVME6100's processor bus interface operates at 133 MHz in MPX mode.

### **Memory Subsystem**

The MVME6100 utilizes a Marvell GT-64360 (Discovery II) system controller to provide the system memory interface as well as various I/O interfaces. The memory interface connects to a dual bank memory subsystem that supports up to 2 GB of DDR system memory when populated with 1 Gigabit memory devices. Although 2 GB of system memory is supported, the initial release of the MVME6100 will have a total of 1 GB of memory implemented with 512 Megabit devices. As the 1 Gigabit devices become more prevalent, future versions of the MVME6100 are planned with a total of 2 GB of system memory. The system memory controller in the Discovery II supports ECC (Error Checking and Correction) allowing detection of double bit errors and correction of single bit errors. The memory subsystem is clocked at a frequency of 133 MHz, but since DDR memory utilizes both edges of the clock, the effective frequency is 266 MHz. Direct accesses to the memory subsystem by the processor, Ethernet, PCI-X or Device Bus interfaces is controlled by an arbiter implemented in the Discovery II Controller which allows for flexibility on an application basis for optimizing and balancing allocation of memory subsystem bandwidth.

### **FLASH Memory**

A total of 128 MB of FLASH memory is supported on the MVME6100 board and is implemented in two 64 MB banks. Each of the FLASH banks has a different write-protection scheme. All of Bank A can be write-protected by a hardware jumper and software control. The upper 1 MB of Bank B can also be write-protected by a hardware jumper and software control. Either FLASH bank can be specified as the boot bank using on-board jumpers.

### **PCI and PMC Interfaces**

The MVME6100 utilizes the Discovery II system controller to implement PCI-X Buses A and B. PCI-X Bus A provides a 32/64-bit data path and is capable of operating in either PCI mode at 33 or 66 MHz or in PCI-X mode at 66 or 100 MHz. The two PMC (PCI Mezzanine Card) sites (PMC 1 and PMC 2) are connected to PCI-X Bus A and support both legacy PMCs as well as the new PCI-X capable PMCs defined in the VITA 39 specification from the VMEbus International Trade Association. Circuitry on the MVME6100 board automatically detects the PCI protocol and frequency capabilities of each of the PMCs and configures the bus to run at the highest common frequency and protocol at which both PMCs are capable of operating. No other onboard devices are connected to PCI-X Bus A in order to minimize loading to ensure that the bus can support up to 100 MHz operation with two PCI-X capable PMCs installed for maximum I/O throughput. Support for PCI-X capable PMCs operating at 100 MHz can provide up to a 50% improvement in I/O performance over conventional PMCs operating at 66 MHz. The PMC 1 connector has 64 I/O pins that are routed to the VMEbus J2 connector on rows A and C while the PMC 2 connector has 46 I/O pins that are routed to the VMEbus J2 connector on rows D and Z. These pins allow PMC I/O signals to be accessed through the rear of a VMEbus chassis using either RTM (Rear Transition Modules) or cables. Adjacent to the PMC 2 connector is an IPMC connector that accommodates the installation of IPMC Modules such as the popular IPMC761. Jumpers on the MVME6100 allow for selection of which IPMC and PMC I/O signals are routed to the P2 connector.

PCI-X Bus B provides a 64-bit data path and operates at 133 MHz. Two devices are connected to PCI-X Bus B, a Tundra Tsi148 PCI-X-to-VME Bridge and a PLX 6520 PCI-X to PCI-X Bridge. The PLX device serves as a bridge between PCI-X Bus B and PCI Bus C and ensures that the slower devices residing on PCI Bus C won't slow down PCI-X Bus B from operating at 133 MHz in PCI-X mode. PCI Bus C provides a PMCSpan interface connector and is capable of 32/64-bit operation at 33/66 MHz. The PMCSpan interface connector allows a PMCSpan Expansion Module with additional PMC sites to be installed on the MVME6100 to provide more I/O connectivity. While current PMCSpan Expansion Modules typically support 32-bit 33 MHz PCI operation, when PCI-X capable PMCSpan Expansion Modules become available in the future, the MVME6100 will be able to support 64-bit 66 MHz operation with them.

### **Ethernet Interfaces**

The MVME6100 implements two full-duplex 10/100/1000 megabit/second Ethernet ports with two front panel RJ45 connectors. Both Ethernet MACs reside in the Discovery II controller while the physical layer for each port is implemented with a Broadcom BCM542S 10/100/1000 BaseT Gigabit transceiver with a SERDES interface. The front panel RJ45 connectors have integrated magnetics as well as link and activity LEDs. One of the Ethernet ports is only accessible from a front panel RJ45 connector, while a jumper is used to configure the second Ethernet port to be accessible from either a front panel RJ45 connector or the VMEbus P2 connector. Having the Ethernet MACs integrated in the Discovery II System Controller offers performance and real estate advantages over utilizing discrete PCI-based Ethernet controllers. The performance advantages are in the areas of greater bandwidth and decreased latency to memory for Ethernet traffic. PCI-based Ethernet controllers incur more latency in that they must first arbitrate for the PCI bus before transferring to and from system memory. Another Ethernet performance advantage can be realized by utilizing the Discovery II's 2 megabit integrated SRAM to store Ethernet descriptors.

### **Serial Interfaces**

Two asynchronous serial ports are provided on the MVME6100. A dual UART device that interfaces to the device bus of the Discovery II serves as the controller for both ports. Signals from one of the serial ports on the dual UART are routed through EIA-232 receivers and transmitters to an RJ45 connector on the front panel. The signals from the second serial port on the dual UART are routed to an on-board header. Both serial ports are capable of signaling at up to 115 Kbaud.

### **VMEbus Interface**

The MVME6100 employs the Tundra Tsi148 PCI-X to VMEbus bridge and TI's SN74VMEH22501 VMEbus transceivers to implement a 2eSST capable VME-64X interface. The Tsi148 was developed by Motorola and is marketed, sold, and supported by Tundra Semiconductor. The PCI-X interface on the Tsi148 operates at 133 MHz on the MVME6100. In addition to the VME interface on this device supporting legacy VME protocols, it also supports the 2eSST VMEbus protocol. "2eSST" stands for Two-Edge Source Synchronous Transfer; "Source Synchronous" means the transmitter sends data along with a strobe and "Two-Edge" indicates that transfers are made on both the rising and falling edges of the strobe. For a write operation, the master is the transmitter and uses DS1\* as the strobe. For a read operation, the slave is the transmitter and uses DTACK\* as the strobe. The MVME6100 uses the 2eSST protocol supported by the Tsi148's VMEbus interface and TI's SN74VMB22501 incident-wave switching transceivers together to achieve up to 320 Mbytes/second transfer rates in properly designed 5-row VMEbus backplanes.

### **Software Support**

The MVME6100 has FLASH-resident firmware that provides POST (Power-On Self-Test), initialization, and the capability to boot a variety of operating systems. Linux support and a VxWorks BSP (Board Support Package) are available for the MVME6100.

### **Summary**

There are many significant performance improvements that the MVME6100 SBC provides over previous generations of VMEbus SBCs while still maintaining backward compatibility. These performance improvements are in the areas of the processor, the memory subsystem, the PCI Buses, the Ethernet interfaces, and the VMEbus interface. Together, they make the MVME6100 a powerful new SBC ready to take on the computational and I/O challenges in today's embedded markets.

### **About the author**

Bob Tufford has spent the last 19+ years designing computer system hardware and software. Bob joined the Motorola Computer Group in 1995 where he is currently a system architect developing next generation product architectures. His previous positions include system architect and lead engineer at Encore Computer Corporation and hardware engineer at Gould Computer Systems Division. Bob holds a Bachelor of Science degree in electrical engineering and a Bachelor of Science degree in chemistry from Florida Atlantic University.

